WHAT IS CLAIMED IS:

1. An encoding device performing run-length encoding and variable-length encoding, comprising:

an input portion for sequentially inputting one block of m×n data;

a comparing and determining portion for determining for each individual data unit input by the input portion whether its value is 0 (zero);

an information register for storing determination result information on the results of the determination by the comparing and determining portion;

a data buffer for storing data input by the input portion;

a read control portion for controlling reading of the data from the data buffer in such a manner that only input data having a value that is not 0 (zero) are read out based on the determination result information stored in the information register;

a run-length encoding portion for performing run-length encoding using data read from the data buffer and the determination result information stored in the information register; and

a variable-length encoding portion for performing variable-length encoding using as a data pair the input data and the number of consecutive data having a value of 0 (zero) that is obtained by the run-length encoding portion.

2. The encoding device according to claim 1,

wherein the determination result information is stored in the information register in a zig-zag scan order with respect to the arrangement of the data in the block.

3. The encoding device according to claim 1, further comprising:

a write control portion for controlling writing of the data to the data buffer;

wherein the write control portion permits writing to the data buffer only if the comparing and determining portion has determined that the value of the data is not 0 (zero).

4. The encoding device according to claim 1,

wherein the data buffer is configured so that it can store L (where L

is a natural number of two or more) input data units per address, and

wherein the encoding device further comprises a selection portion for selecting which of the L input data units that are read from the data buffer should be output to the run-length encoding portion based on the determination result information stored in the information register.

5. The encoding device according to claim 4,

wherein the information register is configured so that it can store m×n bits of determination result information, and

wherein the read control portion reads those L input data from the data buffer only if at least one bit of the determination result information corresponding L input data in the information register indicates that the value of the input data is not 0 (zero).

6. The encoding device according to claim 4,

wherein the selection portion, of the bits of the information register, selects L input data read from the data buffer based on L bits of determination result information corresponding to L input data.

7. The encoding device according to claim 1,

wherein the information register is configured so that it can store m×n bits of determination result information in mutually different arrangement orders, and an information register group is constituted by a plurality of the information registers; and

wherein the encoding device further comprises:

a second input portion for inputting characteristic information indicating block characteristics of the data input by the input portion, and

a register selection portion for selecting any of the information registers of the information register group based on the characteristic information that is input from the second input portion.

8. The encoding device according to claim 2,

comprising an output switching portion having a plurality of process chains, in which one chain is constituted by the information register, the data buffer, the write control portion, and the read control portion, and which controls switching to the data buffer associated with which of the process chains from which to output to the run-length encoding portion;

wherein a process of writing to a data buffer of one of the process chains and a process of reading from a data buffer of another process chain are performed simultaneously.

9. The encoding device according to claim 1,

further comprising a code word number counting portion for counting a number of input data that are not 0 (zero) based on the determination result information of the information register.

10. The encoding device according to claim 9,

further comprising a region setting portion for setting a region within a block that is to be counted by the code word number counting portion.

11. The encoding device according to claim 9,

further comprising a threshold value setting portion for setting a threshold value of the count number of the code word number counting portion and a comparing portion for comparing the count number and the threshold number.

12. The encoding device according to claim 1,

further comprising a final data determination portion for outputting, when it is determined that an input data that is read from the data buffer is the last input data that is not 0 (zero) within the data block based on the determination result information stored in the information register, information indicating that that input data are the final data. to the variable-length encoding portion

13. The encoding device according to claim 1,

further comprising a clock control portion for controlling supply of a clock to the data buffer;

wherein the clock control portion supplies a clock to the data buffer only during a period when the values of the input data are not 0 (zero) based on the determination result information stored in the information register.

14. An encoding device performing run-length encoding and variable-length encoding, comprising:

an input portion for sequentially inputting one block of m×n data;

a processor;

a first processing portion; and

a second processing portion:

wherein the first processing portion includes:

a comparing and determining portion for determining for each individual data unit input by the input portion whether its value is 0 (zero);

a first information register for storing first determination result information on the results of the determination by the comparing and determining portion;

a first data buffer for storing data input by the input portion; and

a write control portion for controlling writing of the data to the first data buffer,

wherein the second processing portion includes:

a second data buffer for storing the second data;

a second information register for storing second determination result information on whether the values of the second data are 0 (zero);

a read control portion for controlling reading of the second data from the second data buffer based on the second determination result information stored in the second information register;

a run-length encoding portion for performing run-length encoding using the second data read from the second data buffer and the second determination result information stored in the second information register; and

a variable-length encoding portion for performing variable-length encoding using as a data pair the second input data and the number of consecutive second input data having a value of 0 (zero) obtained by the run-length encoding portion,

wherein the processor reads the data from the first data buffer based on the information stored in the first information register to create second data,

wherein the read control portion reads only the second data having a value that is not 0 (zero) from the second data buffer based on the second determination result information of the second information register, and

wherein the run-length encoding portion outputs to the variable-length encoding portion, as the number of consecutive second data having a value of 0 (zero), the interval in which the second determination

result information in the second information register indicates that the value of the second data is not 0 (zero).

15. The encoding device according to claim 14,

wherein if the value of a created second data is 0 (zero), then, without outputting that second data, the processor increases the count of the number of second data having a value of 0 (zero), and

wherein if the value of a created second data is not 0 (zero), then the processor outputs the second data and outputs to the run-length encoding portion the number of second data having a value of 0 (zero) that have been counted.

16. An encoding device performing run-length encoding and variable-length encoding, comprising:

an input portion for sequentially inputting one block of m×n data;

a comparing and determining portion for determining for each individual data unit input by the input portion whether its value is 0 (zero);

a data buffer for storing data input by the input portion;

an address storage portion storing addresses in the data buffer of the data that are determined by the comparing and determining portion to have a value that is not 0 (zero);

a read control portion for controlling reading of the input data from the data buffer based on the addresses stored in the address storage portion;

a run-length encoding portion for performing run-length encoding using the input data read from the data buffer and the addresses stored in the address storage portion; and

a variable-length encoding portion for performing variable-length encoding using as a data pair the data and the number of consecutive data having a value of 0 (zero) obtained by the run-length encoding portion;

wherein the read control portion reads only the data having a value that is not 0 (zero) from the data buffer based on the addresses stored in the address storage portion, and

wherein the run-length encoding portion outputs to the variable-length encoding portion, as the number of data units having a value of 0 (zero), the difference between the previous address read from the address storage portion and the current address read from the address storage portion.

17. The encoding device according to claim 16,

wherein the run-length encoding portion calculates, in a zig-zag scan order, a difference between the address read from the data buffer and the address that was read immediately prior, and outputs the difference to the variable-length encoding portion as the number of the data having a value of 0 (zero).

18. The encoding device according to claim 16,

wherein the address storage portion and the read control portion are provided by a processor.

19. An encoding method in which run-length encoding and variable-length encoding are performed, comprising:

a step of sequentially inputting one block of m×n data;

a step of determining for each individual data unit that is input whether its value is 0 (zero);

a step of storing determination result information on the results of the determination to an information register;

a step of storing the input data to a data buffer;

a step of selectively reading data from the data buffer in such a manner that only input data having a value that is not 0 (zero) are read out based on the determination result information stored in the information register;

a step of performing run-length encoding using the data read from the data buffer and the determination result information; and

a step of performing variable-length encoding using as a data pair the data and the number of consecutive data having a value of 0 (zero) obtained in the step of performing run-length encoding.

20. The encoding method according to claim 19,

wherein a buffer that can store L (L is a natural number of two or more) data per address is used as the data buffer; and

wherein the step of selectively reading data from the data buffer includes

a step of selecting which data, of the L data read from the data buffer, to transfer to the run-length encoding process based on the

determination result information stored in the information register, and

a step of transferring the selected data to the run-length encoding process.

21. The encoding method according to claim 19,

wherein the information register is configured so that it can store m×n bits of the determination result information in mutually different arrangement orders, and an information register group constituted by a plurality of the information registers is used;

wherein the encoding method further comprises:

a step of inputting characteristic information showing the block characteristics of the input data, and

a step of selecting an information register from the information register group based on the characteristic information that is input.

22. The encoding method according to claim 19, further comprising:

a step of simultaneously executing a plurality of process chains, each process chain including:

the step of storing the determination result information to the information register;

the step of storing the input data to the data buffer; and

the step of selectively reading data from the data buffer based on the determination results;

and controlling which data read out from the data buffers in what process chain of the plurality of process chains is transferred to the run-length encoding step;

wherein writing to the data buffer in one of the plurality of process chains and reading from a data buffer in another process chain are performed simultaneously.

23. The encoding method according to claim 19, further comprising:

a step of counting a number of input data whose values are not 0 (zero) based on the determination result information in the information register.

24. The encoding method according to claim 23, further comprising:

a step of setting a region within one block to be subjected to the

counting.

25. The encoding method according to claim 23, further comprising:

a step of setting a threshold value of a count number; and

a step of comparing the count number and the threshold value.

26. The encoding method according to claim 19, further comprising:

a step of determining whether an input data that is read from the data buffer is a last input data that is not 0 (zero) within the data block, based on the determination result information stored in the information register;

wherein when it is determined that the input data are the last input data that is not 0 (zero), then information indicating that the input data are final data is transferred to the variable-length encoding step.

27. The encoding method according to claim 19, comprising:

a step of controlling a clock supplied to the data buffer;

wherein based on determination result information stored in the information register, a clock is supplied to the data buffer only during a period of data whose values are not 0 (zero).

28. An encoding method in which run-length encoding and variable-length encoding are performed, comprising:

a first process step including:

a step of sequentially inputting one block of m×n data;

a step of determining whether a value of each unit of data that is input is 0 (zero);

a step of storing determination result information on the results of the determination to a first information register; and

a step of storing the input data to a first data buffer; and

a second process step including:

a step of reading the data from the first data buffer based on the determination result information stored in the first information register to create second data;

a step of storing the second data to a second data buffer;

a step of storing second determination result information on whether the values of the second data are 0 (zero) to a second information

register;

a step of controlling reading of the second data from the second data buffer based on the second determination result information stored in the second information register;

a step of performing run-length encoding using the second data read from the second data buffer and the second determination result information stored in the second information register; and

a step of performing variable-length encoding using as a data pair the second input data and the number of consecutive second input data having a value of 0 (zero) obtained in the step of performing run-length encoding;

wherein only the second data having a value that is not 0 (zero) based on the second information register are read from the second data buffer, and

wherein in the run-length encoding step, an interval in which the second determination result information in the second information register indicates that the value of the second data is not 0 (zero) is transferred to the step of performing variable-length encoding as the number of consecutive second data having a value that is 0 (zero).

29. An encoding method in which run-length encoding and variable-length encoding are performed, comprising:

a step of sequentially inputting one block of m×n data;

a step of determining whether a value of each unit of the input data is 0 (zero);

a step of storing the input data to a data buffer;

a step of storing addresses in the data buffer of the data that are determined to have a value that is not 0 (zero) to an address storage portion;

a step of reading the data from the data buffer based on the addresses stored in the address storage portion;

a step of performing run-length encoding using the data read from the data buffer and the addresses that are stored; and

a step of performing variable-length encoding using as a data pair the data and the number of consecutive data having a value of 0 (zero) obtained in the step of performing run-length encoding;

wherein only input data having a value that is not 0 (zero) based on the addresses stored in the storage portion are read from the data buffer,

and the difference between the previously read address and the currently read address is transferred to the step of performing variable-length encoding as the number of input data having a value of 0 (zero).

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